

**Semester I**

<b>Code</b>	<b>Subject</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
ECE 5101	Physical Electronics	3	0	0	3
ECE 5102	Advanced Digital System Design	3	0	0	3
ECE 5103	Embedded Networked Systems Design	3	0	0	3
ECE 5104	Mixed Signal IC design	3	0	0	3
ECE 5105	MEMS	3	0	0	3
ECE XXXX	Elective I	3	0	0	3
ECE 5181	VLSI Design Laboratory I	0	0	3	2
	Total	18	0	3	20

**Semester II**

<b>Code</b>	<b>Subject</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
ECE 5106	Foundations of VLSI CAD	3	0	0	3
ECE 5107	RF Microelectronics Chip design	3	0	0	3
ECE 5108	System On Chip Design	3	0	0	3
ECE 5109	DSP Architecture	3	0	0	3
ECE 5110	Testing of VLSI Circuits	3	0	0	3
ECE XXXX	Elective-II	3	0	0	3
ECE 5182	VLSI Design Laboratory II	0	0	3	2
	Total	18	0	3	20

**Semester III**

<b>Code</b>	<b>Subject</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
ECE XXXX	Elective III	3	0	0	3
ECE XXXX	Elective IV	3	0	0	3
ECE XXXX	Elective V	3	0	0	3
ECE 6198	Project Work Phase I	-	-	18	6
	Total	9	0	18	15

**Semester IV**

<b>Code</b>	<b>Subject</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
ECE 6199	Project Work Phase II	-	-	36	12
	Total	-	-	36	12

**ELECTIVES**

<b>Code</b>	<b>Subject</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
ECE 5111	Optimization Techniques	3	0	0	3
ECE 5112	Low Power VLSI Design	3	0	0	3
ECE 5113	Analog VLSI Design	3	0	0	3
ECE 5114	Design of Semiconductor Memories	3	0	0	3
ECE 5115	VLSI Digital Signal Processing Systems	3	0	0	3
ECE 5116	Physical Design of VLSI Circuits	3	0	0	3
ECE 5117	Image processing	3	0	0	3
ECE 5118	Nanoelectronics	3	0	0	3
ECE 5119	Microwave Integrated Circuits	3	0	0	3
ECE 5120	VLSI Technology	3	0	0	3
ECE 6101	Designing with ASICs	3	0	0	3
ECE 6102	FPGA based System Design	3	0	0	3
ECE 6103	Advanced Computer Architecture	3	0	0	3
ECE 6104	Fuzzy Logic and Neural Networks	3	0	0	3
ECE 6105	Genetic Algorithms and VLSI Design Application	3	0	0	3
ECE 6106	System Design	3	0	0	3
ECE 6107	Communication networks	3	0	0	3
ECE 6108	Signal processing and smart antennas for wireless communication	3	0	0	3
ECE 6109	Low Power Processors and SOCs	3	0	0	3
ECE 6110	VLSI Signal Processing and Techniques	3	0	0	3

<b>SEMESTER I</b>
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<b>ECE 5101</b>	<b>PHYSICAL ELECTRONICS</b>	L	T	P	C
		3	0	0	3

**REVIEW OF QUANTUM MECHANICS**

Electrons in periodic lattices, E-k diagrams, Quasiparticles in semiconductors, electrons, holes and phonons. Boltzmann transport equation and solution in the presence of low electric and magnetic fields - mobility and diffusivity - Carrier statistics - Continuity equation, Poisson's equation and their solution.

**HIGH FIELD EFFECTS OF TRANSISTORS**

Velocity saturation, hot carriers and avalanche breakdown. Schottky, homo- and hetero-junction band diagrams and I-V characteristics, and small signal switching models- two terminal and surface states devices based on semiconductor junctions. Semiconductor surfaces- The ideal and non-ideal MOS capacitor band diagrams and CVs - Effects of oxide charges, defects and interface states.

**CHARACTERIZATION OF MOS CAPACITORS**

HF and LF CVs, avalanche injection- High field effects and breakdown. Four probe and Hall measurement - CVs for dopant profile characterization - Capacitance transients and DLTS.

**MOS MODELS AND ITS CARRIER EFFECTS**

Pao-Sah and Brews models - Short channel effects in MOS transistors. Hot-carrier effects in MOS transistors - Quasi-static compact models of MOS transistors - Measurement of MOS transistor parameters - Scaling and transistors structures for ULSI.

**MODELING OF TRANSISTORS AND CHARACTERISTICS**

Silicon-on-insulator transistors - High-field and radiation effects in transistors. Ebers-Moll model charge control model - small-signal and switching characteristics - Graded-base and graded-emitter transistors- High-current and high- frequency effects Hetero-junction bipolar transistors- Junction FETs JFET, MESFET and hetero-junction FET.

**REFERENCES**

1. Arora. N. D., MOSFET Models for VLSI Circuit Simulation, Springer-Verlag, 1993.
2. Roulston. E. J., Bipolar Semiconductor Devices, McGraw-Hill, 1990.
3. Sze. M., Physics of Semiconductor Devices, Wiley Eastern, 2<sup>nd</sup> edition, 1981.
4. Tsividis. Y. P., Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
5. Takeda, Hot-carrier Effects in MOS Transistors, Academic Press, 1995.
6. McKelvey. J. P., introduction to Solid State and Semiconductor Physics, Harper and Row and John Weathe Hill, 1966.

<b>ECE 5102</b>	<b>ADVANCED DIGITAL SYSTEM DESIGN</b>	L	T	P	C
		3	0	0	3

**ANALYSIS OF CLOCKED SYNCHRONOUS SEQUENTIAL NETWORKS (CSSN)**

Modelling of CSSN State Stable Assignment and Reduction, Design of CSSN, Design of Iterative Circuits, ASM Chart, and ASM Realization.

**STATIC AND DYNAMIC CMOS DESIGN, OPTIMIZATION TECHNIQUES**

Combinational circuit design, circuit families, static CMOS, ratioed circuits, Cascade voltage switch logic, Dynamic circuits. Pass transistor circuits, Differential circuits. Combinational

network delay. Power and energy optimization sequential machine design styles. Rules for clocking. Performance analysis.

### **ANALYSIS OF ASYNCHRONOUS SEQUENTIAL CIRCUIT (ASC)**

Flow Table Reduction, Races in ASC, State Assignment, Problem and the Transition Table , Design of ASC, Static and Dynamic Hazards, Essential Hazards, Designing Vending Machine Controller. Mixed Operating Mode Asynchronous Circuits, Sequencing static circuits, Circuit design of latches and flip-flops, Static sequencing element methodology, Sequencing dynamic circuits, Synchronizers.

### **PROGRAMMABLE LOGIC DEVICES (PLDS)**

Programmable gate arrays, Realization State machine using PLD, EPROM to Realize a Sequential Circuit, Designing a Synchronous Sequential Circuit using a GAL, EPROM. Xilinx series FPGAs, Altera complex PLDs, Altera Flex 10K series CPLDs, FPGA based system design, FPGA fabrics.

### **DATAPATH AND ARRAY SUBSYSTEMS**

Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context-addressable memory.

### **REFERENCES**

1. Donald G. Givone, Digital principles and Design, Tata McGraw Hill, 2002.
2. John M. Yarbrough, Digital Logic applications and Design, Thomson Learning, 2001.
3. Nripendra N. Biswas, Logic Design Theory, Prentice Hall of India, 2001.
4. Charles H. Roth Jr., Fundamentals of Logic design, Thomson Learning, 2004.
5. Weste etal. N.H.E., CMOS VLSI Design, Pearson Education, 3<sup>rd</sup> Edition 2005.
6. Wolf. W., FPGA- based System Design, Pearson Education, 2004.

<b>ECE 5103</b>	<b>EMBEDDED NETWORKED SYSTEMS DESIGN</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

### **NETWORK SYSTEMS**

Embedded network systems , Representation of Signals , Signal propagation.

### **INSTRUMENTATION CONCEPTS**

Sensor principles - Source detection & Identification.

### **COMMUNICATION AND NETWORKING**

Digital communication - Multiple source estimation & multiple access communication - Networking - Network position & synchronization services.

### **MANAGEMENT AND NODE ARCHITECTURE**

Energy management - Data management - Articulation mobility & infrastructure - Node architecture, Network data integrity.

### **EXPERIMENTAL DESIGN**

Experimental systems design - Ethical, legal & social implication of ENS – Design principles for ENS

### **REFERENCES**

1. Gregory Pottie, William Kaiser, Principles of Embedded Networked Systems Design, Cambridge University Press, 2005.

<b>ECE 5104</b>	<b>MIXED SIGNAL IC DESIGN</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

**DATA CONVERTER MODELLING**

Sampling and aliasing, SPICE models for DAC, ADCs, Quantization noise.

**DATA CONVERTER SNR**

Overview, Improving SNR using Averaging, Using feedback to improve SNR.  
Noise shaping Data Converters- Noise shaping fundamentals, Noise shaping topologies.

**SUBMICRON CMOS CIRCUIT DESIGN**

Overview and models, Digital circuit design, Analog circuit design.

**IMPLEMENTATION OF DATA CONVERTERS**

R-2R Topologies for DACs, Op-Amp in Data Converters, Implementing DACs

**INTEGRATOR- BASED CMOS FILTERS**

Building Blocks, Filtering topologies, filters using Noise- shaping, Push-pull amplifier, 1st order Noise shaping modulator, measuring 1/F noise, discrete analog integrator, quantization noise.

**REFERENCES**

1. Jacob Baker.R., CMOS Mixed signal circuit design, Wesley – IEEE, 2000.
2. Allen Holberg, CMOS Analog Circuit Design, PHI
3. Baker, CMOS Circuit Design, Layout and Simulation, Wiley

<b>ECE 5105</b>	<b>MEMS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

**HISTORICAL BACKGROUND**

Silicon Pressure sensors, Micromachining, Micro-Electro Mechanical Systems

**MICROFABRICATION AND MICROMACHINING**

Integrated Circuit Processes, Bulk Micro-machining- Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA)

**PHYSICAL MICROSENSORS**

Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples- Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors

**MICROACTUATORS**

Electromagnetic and Thermal micro-actuation, Mechanical design of micro-actuators, Micro-actuator examples, micro-valves, micro-pumps, micro-motors, Micro-actuator systems, Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector

**SURFACE MICROMACHINING**

One or two sacrificial layer processes, Surface micromachining requirements, Poly-silicon surface micromachining, other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micro-machined Systems - Success Stories, Micro-motors, Gear trains, Mechanisms

Application Areas- All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays.

#### REFERENCES

1. Stephen D. Senturia, Microsystem Design, Kluwer Academic Publishers, 2001.
2. Marc Madou, Fundamentals of Micro-fabrication, CRC Press, 1997.
3. Gregory Kovacs, Micro-machined Transducers Sourcebook, WCB McGraw-Hill, Boston, 1998.
4. Bao.M.H., Micromechanical Transducers- Pressure sensors, accelerometers, and gyroscopes, Elsevier, New York, 2000.

<b>ECE 5181</b>	<b>VLSI DESIGN LABORATORY - I</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	3	2

#### 1. SIMULATION AND SYNTHESIS OF COMBINATIONAL AND SEQUENTIAL CIRCUITS

Encoders and Decoders  
Code Converters  
Universal Shift Registers  
Universal counters  
State machine realization

#### 2. FPGA IMPLEMENTATION OF SEQUENTIAL CIRCUITS

Counters  
Shift Registers  
State machines  
MAC Unit

#### 3. SPICE IMPLEMENTATION OF ANALOG AND DIGITAL CIRCUITS

Amplifiers  
Differentiators and Integrators  
Multivibrators

#### 4. MANUAL LAYOUT DESIGN OF SIMPLE DIGITAL CIRCUITS USING ANALOG DESIGN ENVIRONMENT IN CADENCE

Universal gates  
Multiplexers  
Flip flops

### SEMESTER II

<b>ECE 5106</b>	<b>FOUNDATIONS OF VLSI CAD</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

#### MATRICES

Linear dependence of vectors, solution of linear equations, bases of vector spaces, orthogonality, complementary orthogonal spaces and solution spaces of linear equations.

#### GRAPHS

Representation of graphs using matrices- Paths, connectedness- circuits, cut-sets, trees- Fundamental circuit and cut-set matrices-

#### VOLTAGE AND CURRENT SPACES

Voltage and current spaces of a directed graph and their complementary orthogonality.

**ALGORITHMS**

Efficient representation of graphs- Elementary graph algorithms involving BFS and DFS trees, such as finding connected and 2- connected components of a graph, the minimum spanning tree, shortest path between a pair of vertices in a graph-

**DATA STRUCTURES**

Data structures such as stacks, linked lists and queues, Binary trees and heaps. Time and space complexity of algorithms.

**REFERENCES**

1. Hoffman. K. and Kunze. R.E., Linear Algebra, Prentice Hall (India), 1986.
2. Balabanian. N. and Bickart. T. A., Linear Network Theory Analysis, Properties, Design and Synthesis, Matrix Publishers Inc., 1981.
3. Cormen. T., et. al., Algorithms, MIT Press and McGraw-Hill, 1990.

<b>ECE 5107</b>	<b>RF MICROELECTRONICS CHIP DESIGN</b>	L	T	P	C
		3	0	0	3

**RF AND WIRELESS TECHNOLOGY**

Complexity, design and applications. Choice of Technology.

**BASIC CONCEPTS IN RF DESIGN-**

Nonlinearly and Time Variance, inter-symbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion.

**ANALOG AND DIGITAL MODULATION FOR RF CIRCUITS**

Comparison of various techniques for power efficiency. Coherent and Non coherent deflection. Mobile RF Communication systems and basics of Multiple Access techniques. Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters. BJT and MOSFET behavior at RF frequencies modeling of the transistors and SPICE models. Noise performance and limitation of devices. Integrated Parasitic elements at high frequencies and their monolithic implementation.

**BASIC BLOCKS IN RF SYSTEMS AND THEIR VLSI IMPLEMENTATION**

Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers and their working and implementations.

**OSCILLATORS**

Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonatorless VCO design. Quadrature and single-sideband generators  
Radio Frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifiers design. Linearization techniques, Design issues in integrated RF filters.

**RF MEMS**

Introduction to RF MEMS, Design of MEMS Switch circuits, micro machined inductors, reconfigurable MEMS Networks, Phase shifters, Oscillators

**REFERENCES**

1. Razavi. B., RF Microelectronics, Prentice-Hall PTR, 1998.
2. Lee. T. H., The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, 1998.
3. Jacob Baker. R., CMOS Circuit Design, Layout and Simulation, Prentice-Hall of India, 1998.

4. Tsividis. Y. P., Mixed Analog and Digital VLSI Devices and Technology, McGraw Hill, 1996.
5. Gabriel M. Rabeiz, RF MEMS, Theory, design and Technology, Wiley 2003

<b>ECE 5108</b>	<b>SYSTEM ON CHIP DESIGN</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

#### **SYSTEM LEVEL DESIGN**

System level design-Tools & methodologies for system level design, System level space & modeling languages, SOC block based design & IP assembly, Performance evaluation methods for multiprocessor SOC design,

#### **POWER MANAGEMENT AND SYNTHESIZING**

System level power management, Processor modeling & design tools, Embedded software modeling & design Using performance metrics to select microprocessor for IC design, Parallelizing High-Level Synthesize ,A code transformational approach to High Level Synthesize.

#### **MICRO-ARCHITECTURE DESIGN AND POWER OPTIMIZATION**

Micro-architecture design, Cycle accurate system – level modeling, Performance evaluation, Micro architectural power estimation optimization, Design planning.

#### **SOFTWARE DESIGN VERIFICATION**

logical verification, Design & Verification languages, Digital simulation, using transactional, level models in an SOC design, Assertion based verification.

#### **HARDWARE DESIGN VERIFICATION**

Hardware acceleration & emulation, Formal property verification, TEST, DFT, ATPG, Analog & mixed signal test

#### **TEXT BOOK**

1. Louis Scheffer Luciano Lavagno and Grant Martin, EDA for IC System verification and Testing, CRC, 2006.

<b>ECE 5109</b>	<b>DSP ARCHITECTURES</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

#### **DSP ALGORITHMS AND APPLICATIONS**

Computational characteristics of DSP algorithms and applications- their influence on defining a generic instruction-set architecture for DSPs.

#### **ARCHITECTURAL REQUIREMENT OF DSPs**

High throughput, low cost, low power, small code size, embedded applications, Techniques for enhancing computational throughput parallelism and pipelining.

#### **DATA-PATH OF DSPs**

Multiple on-chip memories and buses, dedicated address generator units, specialized processing units (hardware multiplier, ALU, shifter) and on-chip peripherals for communication and control.

#### **CONTROL-UNIT OF DSPs**

Pipelined instruction execution, specialized hardware for zero-overhead looping, interrupts.

**FIXED-POINT AND FLOATING POINT DSPs**

Brief description of TMS320 C5x /C54x/C3x DSPs- Programmer's model. Architecture of Analog Devices fixed-point and floating-point DSPs- brief description of ADSP 218x / 2106x DSPs- Programmer's model.

Advanced DSPs- TI's TMS 320C6x, ADI's Tiger-SHARC, Lucent Technologies' DSP 16000 VLIW processors. Applications- a few case studies of application of DSPs in communication &multimedia.

**REFERENCES**

1. Pirsch. P., Architectures for Digital Signal Processing, John Wiley, 1999.
2. Higgins. R. J., Digital Signal Processing in VLSI, Prentice-Hall, 1990.
3. Texas Instruments TMS320C5x, C54x and C6x Users Manuals. Analog Devices ADSP 2100 - family and 2106x-family Users Manuals.
4. Parhi. K., VLSI Digital Signal Processing Systems, John Wiley, 1999.
5. Parhi. K. and Nishitani. T., Digital Signal Processing for Multimedia Systems, Marcel Dekker, 1999.

<b>ECE 5110</b>	<b>TESTING OF VLSI CIRCUITS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

**TESTING**

Fault table method , path sensitization method, boolean difference method, kohavi Algorithm, tolerance techniques, compact algorithm, practical PLA's, fault in PLA test generation, masking cycle , DFT schemes, built-in self test. Faults and their manifestations. Combinational logic and fault simulation.

**FAULT MODELS AND DFT**

Scope of testing and verification in VLSI design process, Issues in test and verification of complex chips, embedded cores and SOCs, Fundamentals of VLSI testing, Fault models, Automatic test pattern generation, Design for testability, Scan design, Test interface and boundary scan, System testing and test for SOCs, IDDQ testing, Delay fault testing.

**DESIGN VERIFICATION TECHNIQUES**

BIST for testing of logic and memories, Test automation. Design verification techniques based on simulation, analytical and formal approaches. Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking.

**HARDWARE EMULATION**

Structural and non-structural test generation techniques. Combinational ATPG, Current sensing based testing, Classification of sequential ATPG methods, Fault collapsing and simulation Test generation for synchronous and asynchronous circuits.

**TEST COMPACTION**

Universal test, Pseudo-exhaustive and iterative logic array testing, Clocking schemes for delay fault testing, Design for testability- Scan design, use of scan chains,

**REFERENCES**

1. Bushnell. M. and Agrawal. V. D., Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers, 2000.
2. Abramovici. M., Breuer. M. A. and Friedman. A. D., Digital Systems Testing and Testable Design, IEEE Press, 1990.
3. Kropf. T., Introduction to Formal Hardware Verification, Springer Verlag, 2000.

4. Abramovici. M., Digital System Testing and Testable Design, Computer Science Press, 1990.

<b>ECE 5182</b>	<b>VLSI DESIGN LABORATORY II</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	3	2

1. Automatic Layout Design of Systems using Cadence- SOC52 – Encounter
2. Net list Generation using Cadence- SOC52 - Build Gates
3. Design of Elevator Controller using ARM Processor
4. Design of Model Train Controller using ARM Processor
5. Design and Implementation of ALU on FPGA
6. Design and Implementation of RISC processor on FPGA

<b>ELECTIVES</b>
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<b>ECE 5111</b>	<b>OPTIMIZATION TECHNIQUES</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

**LINEAR PROGRAMMING**

Formulation, Graphical and simplex methods, Big-M method, two phase method, Dual simplex method, Primal Dual problems.

**UNCONSTRAINED TECHNIQUES**

Necessary and sufficient conditions, unrestricted search method, Fibonacci and Golden section method,

**QUADRATIC INTERPOLATION**

Cubic interpolation and direct root methods. Unconstrained n dimensional optimization techniques, direct search methods, Random search method.

**PATTERN SEARCH METHODS**

Rosenbrock's method, Descent methods, Steepest descent, conjugate gradient, Quasi - Newton methods. Constrained optimization Techniques,

**NECESSARY CONDITIONS**

Equality and inequality constraints, Kuhn-Tucker conditions, Gradient projection method-cutting plane method, penalty function method. Dynamic programming, Principle of optimality, recursive equation approach, application to shortest route, cargo-loading, allocation and production schedule problems.

**REFERENCES**

1. Fox. R. L., Optimization methods for Engineering Design, Addition Wesley.
2. Rao. S. S., Optimization- Theory and Application, Wiley Eastern Press, Halsted Press, 2<sup>nd</sup> Edition.
3. Taha. H. A., Operations Research- An Introduction, Prentice Hall of India.

<b>ECE 5112</b>	<b>LOW POWER VLSI DESIGN</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

### **EVOLUTION OF CMOS, BICMOS TECHNOLOGY**

Evolution of CMOS technology 0.25  $\mu\text{m}$  and 0.1  $\mu\text{m}$  technologies, Shallow trench isolation, Lightly-doped drain, Buried channel, Bi-CMOS and SOI CMOS technologies. Second order effects and capacitance of MOS devices CMOS inverters, static logic circuits of CMOS, pass transistor, Bi-CMOS, SOI CMOS and low power CMOS techniques.

### **DYNAMIC LOGIC CIRCUITS AND HIERARCHY LIMITS**

Basic concepts of dynamic logic circuits, various problems associated with dynamic logic circuits. Differential, Bi-CMOS and low voltage dynamic logic circuits.

Different types of memory circuits. Adder circuits, Multipliers, advanced structures. PLA, PLL, Processing unit, Hierarchy of limits of power, Sources of power consumption.

### **PRINCIPLES OF LOW POWER DESIGN AND OPTIMIZATION TECHNIQUES**

Physics of power dissipation in CMOS FET devices- Basic principle of low power design. Logical level power optimization, Circuit level low power design, Circuit techniques for reducing power consumption in adders and multipliers.

### **ADVANCED AND ARITHMETIC TECHNIQUES**

Computer Arithmetic techniques for low power systems, reducing power consumption in memories, Low power clock, Interconnect and layout design, advanced techniques, Special techniques.

### **POWER ESTIMATION TECHNIQUES AND SOFTWARE DESIGN**

Power estimation techniques, Logic level power estimation, Simulation power analysis, and probabilistic power analysis. Synthesis for low power, Behavioral level transforms, Software design for low power.

### **REFERENCES**

1. Kuo. J. B. and Lou. J. H., Low-voltage CMOS VLSI Circuits, Wiley, 1999.
2. Roy. K. and Prasad . S. C., LOW POWER CMOS VLSI circuit design, Wiley, 2000
3. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, Designing CMOS Circuits For Low Power, Kluwer, 2002.
4. Kuo. B. and Lou. J. H., Low voltage CMOS VLSI Circuits, Wiley, 1999.
5. Chandrakasan.A.P. and Broadersen.R.W., Low power digital CMOS design, Kluwer, 1995.
6. Gary Yeap, Practical low power digital VLSI design, Kluwer, 1998.
7. Abdellatif Bellaouar, Mohamed Elmasry.I., Low power digital VLSI design, Kluwer, 1995.
8. James B. Kuo, Shin – chia Lin, Low voltage SOI CMOS VLSI Devices and Circuits, John Wiley and Sons inc., 2001.

<b>ECE 5113</b>	<b>ANALOG VLSI</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

### **ADVANCED MOS MODELING, BJT MODELING**

Common Source, Common Drain and Common Gate amplifiers. Current mirrors – active loads. High input impedance current mirrors. BJT gain stages.

**CMOS OPERATIONAL AMPLIFIERS AND DATA CONVERTERS**

CMOS operational amplifiers - compensation. Comparators, Sample and hold circuits MOS, CMOS and Bi CMOS S/H circuits. Switched capacitor filters, operation, analysis and applications. Nyquist rate. D/A converters. A/D converters. Over sampling techniques, filter design.

**INTRODUCTION TO ANALOG VLSI AND MIXED SIGNAL ISSUES IN CMOS TECHNOLOGIES**

Basic MOS models, SPICE Models and frequency dependent parameters. Basic MNOS/CMOS gain stage, cascade and cascade circuits. Frequency response, stability and noise issues in amplifiers.

**CMOS ANALOG BLOCKS**

Current Sources and Voltage references, Differential amplifier and OPAMP design, Frequency Synthesizers and Phased lock-loop.

**NON-LINEAR ANALOG BLOCKS**

Comparators, Charge-pump circuits and Multipliers, Data converters, Analog Interconnects. Analog Testing and Layout issues, Low Voltage and Low Power Circuits, Introduction to RF Electronics, Basic concepts in RF design

**REFERENCES**

1. Jacob Baker.R., Li.H.W., and Boyce.D.E., CMOS Circuit Design ,Layout and Simulation, Prentice-Hall of India,1998.
2. Mohammed Ismail and Terri Faiz, Analog VLSI Signal and Information Process, McGraw-Hill Book company,1994.
3. Paul R. Gray and Meyer.R.G., Analysis and design of Analog Integrated circuits, John Wiley and Sons inc., USA, 3<sup>rd</sup> Edition, 1993.
4. John.D.A. and Martin. K., Analog Integrated Circuit Design, Wiley, 1997.
5. Razavi.B., RF Microelectronics, Prentice-Hall PTR,1998

<b>ECE 5114</b>	<b>DESIGN OF SEMICONDUCTOR MEMORIES</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

**RANDOM ACCESS MEMORY TECHNOLOGIES**

STATIC RANDOM ACCESS MEMORIES (SRAMs)- SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.

**DYNAMIC RANDOM ACCESS MEMORIES (DRAMs)**

DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures-Bi-CMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

**NONVOLATILE MEMORIES**

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Read-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

**MEMORY FAULT MODELING, TESTING**

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Non-volatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing

**SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS**

General Reliability Issues-RAM Failure Modes and Mechanism-Non-volatile Memory Reliability-Reliability Modelling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures.

**PACKAGING TECHNOLOGIES**

Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magneto-resistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

**REFERENCES**

1. Ashok K. Sharma, Semiconductor Memories- Technology, Testing, and Reliability, Wiley-IEEE Press, 2002.
2. Ashok K. Sharma, Semiconductor Memories, Two-Volume Set, Wiley-IEEE Press, 2003.
3. Ashok K. Sharma, Semiconductor Memories- Technology, Testing, and Reliability, Prentice Hall of India, 1997.
4. Brent Keeth, R. Jacob Baker, DRAM Circuit Design- A Tutorial, Wiley-IEEE Press, 2000.
5. Betty Prince, High Performance Memories- New Architecture DRAMs and SRAMs – Evolution and Function, Wiley, 1999.

<b>ECE 5115</b>	<b>VLSI DIGITAL SIGNAL PROCESSING SYSTEMS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

**INTRODUCTION TO DSP SYSTEMS**

Introduction-Typical DSP algorithms- Iteration Bound – data flow graph representations, loop and iteration bound, Longest path Matrix algorithm- Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power

**RETIMING**

Retiming - definitions and properties- Transformations. Folding and unfolding DSP programs, Unfolding – algorithm, properties, sample period reduction and parallel processing application- Algorithmic strength reduction in filters and transforms – 2-parallel FIR and fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, and parallel rank-order filters.

**FAST CONVOLUTION**

Fast convolution – Cook-Toom and modified Cook-Toom algorithm- Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look-Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition, Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed

look-ahead, pipelined LMS adaptive filter.

### **BIT-LEVEL ARITHMETIC ARCHITECTURES**

Scaling and round off noise- scaling operation, round off noise, state variable description of digital filters, scaling and round off noise computation, round off noise in pipelined first-order filters- Bit-Level Arithmetic Architectures- parallel multipliers-sign extension, carry - ripple array, carry-save, 4x 4 bit Baugh- Wooley carry-save tabular form and implementation, interleaved floor plan and bit plan based digital filters , design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, distributed arithmetic.

### **PROGRAMMING DIGITAL SIGNAL PROCESSORS**

Redundant arithmetic and number representations, carry free radix 2 addition and subtraction, Hybrid radix 4 addition, hybrid Radix 2 redundant multiplication architectures, data format conversion, Redundant to non redundant converter, Numerical Strength Reduction – sub expression elimination, multiple constant multiplications, iterative matching. Linear transformations- Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs, clock skew in edge-triggered single-phase clocking, two-phase clocking, Synchronous pipelining and clocking styles, Wave pipelining, constraint space diagram and degree of wave pipelining. Implementation of wave-pipelined systems, asynchronous pipelining bundled data versus dual rail protocol- Programming Digital Signal Processors – general architecture- Low power Design – needs for low power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design, Scaling versus power consumption, Power analysis, power reduction and estimation techniques, Low power IIR and CMOS lattice filter

### **REFERENCES**

1. Keshab K. Parhi, VLSI Digital Signal Processing systems, Design and implementation, Wiley, Inter Science, 1999.
2. Gary Yeap, Practical Low Power Digital VLSI Design, Kluwer Academic Publishers, 1998.
3. Mohammed Ismail and Terri Fiez, Analog VLSI Signal and Information Processing, Mc Graw-Hill, 1994.
4. Kung. S. Y., White House. H. J., T. Kailath, VLSI and Modern Signal Processing, Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, Design of Analog and Digital VLSI Circuits for Telecommunication and Signal Processing, Prentice Hall, 1994.

<b>ECE 5116</b>	<b>PHYSICAL DESIGN OF VLSI CIRCUITS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

### **VLSI TECHNOLOGY**

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein-Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms

### **PLACEMENT USING TOP-DOWN APPROACH**

Partitioning- Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic- Ratio-cut - partition with capacity and i/o constraints.

Floor planning- Rectangular dual floor planning- hierarchical approach- simulated annealing- Floor plan sizing. Placement- Cost function- force directed method- placement by simulated

annealing- partitioning placement- module placement on a resistive network – regular placement - linear placement.

### **ROUTING USING TOP DOWN APPROACH**

Fundamentals- Maze running- line searching- Steiner trees.

Global Routing- Sequential Approaches- hierarchical approaches- multi-commodity flow based techniques- Randomized Routing- One Step approach- Integer Linear Programming.

Detailed Routing- Channel Routing, Switch box routing. Routing in FPGA- Array based FPGA- Row based FPGAs.

### **PERFORMANCE ISSUES IN CIRCUIT LAYOUT**

Delay Models- Gate Delay Models- Models for interconnected Delay- Delay in RC trees.

Timing – Driven Placement- Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Driving Routing- Delay Minimization- Clock Skew Problem- Buffered Clock Trees. Minimization- constrained via Minimization- unconstrained via Minimization- Other issues in minimization.

### **SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION**

Planar subset problem (PSP) - Single layer global routing- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing- Multiple chip modules (MCM)- Programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

### **REFERENCES**

1. Sarafzadeh, C.K. Wong, An Introduction to VLSI Physical Design, Mc Graw Hill International Edition 1995
2. Preas M. Lorenzatti, Physical Design and Automation of VLSI systems, The Benjamin Cummins Publishers, 1998.
3. Ban Wong, Anurag Mittal, Yu Cao, Greg Starr, Nano CMOS Circuit and Physical Design, Wiley, John & Sons inc., 2004.
4. Naveed A. Sherwani, Algorithm for VLSI Physical Design Automation , Springer, 3<sup>rd</sup> Edition, 1998.
5. Sadiq M. Sait, Habib Youssef, VLSI Physical Design Automation, Theory and Practice World Scientific Publishing Company, 1<sup>st</sup> Edition, 1999.
6. Bryan T. Preas, Michael Lorenzetti, Physical Design Automation of VLSI system, Benjamin – Cummings Pub. Co, 1998.

<b>ECE 5117</b>	<b>IMAGE PROCESSING</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
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### **IMAGE REPRESENTATION**

Gray scale and colour Images, image sampling and quantization. Two dimensional orthogonal transforms - DFT, FFT, WHT, Haar transform, KLT, DCT.

### **IMAGE ENHANCEMEN**

Filters in spatial and frequency domains, histogram-based processing, homo-morphic filtering. Edge detection - non parametric and model based approaches, LOG filters, localisation problem. Image Restoration - PSF, circulant and block - circulant matrices, deconvolution, restoration using inverse filtering, Wiener filtering and maximum entropy-based methods.

### **MATHEMATICAL MORPHOLOGY**

Binary morphology, dilation, erosion, opening and closing, duality relations, gray scale morphology, applications such as hit-and-miss transform, thinning and shape decomposition.

**COMPUTER TOMOGRAPHY**

Parallel beam projection, Radon transform, and its inverse, Back-projection operator, Fourier-slice theorem, CBP and FBP methods, ART, Fan beam projection. Image communication - JPEG, MPEGs and H.26x standards, packet video, error concealment.

**IMAGE TEXTURE ANALYSIS**

Co-occurrence matrix, measures of textures, statistical models for textures. Misc. topics such as - Hough Transform, boundary detection, chain coding, and segmentation, thresholding methods.

**REFERENCES**

1. Jain. A. K. , Fundamentals of digital image processing, Prentice Hall of India, 1989.
2. Haralick. R. M., and Shapiro. L. G., Computer and Robot Vision, Vol-1, Addison Wesley, Reading, MA, 1992.
3. Jain. R., Kasturi. R. and Schunck. B. G., Machine Vision, McGraw-Hill International Edition, 1995.
4. Pratt. W. K., Digital image processing, Prentice Hall, 1989.
5. Rosenfold. A. and Kak. A. C., Digital image processing, Vols. 1 and 2, Prentice Hall, 1986.
6. Andrew. H. C., and Hunt. B. R., Digital image restoration, Prentice Hall, 1977

<b>ECE 5118</b>	<b>NANOELECTRONICS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

**BASIC ELECTRONICS**

Atom, Molecular and Crystal structures. Atomic numbers, operation of Diodes, transistors, Energy gap, Quasiparticles in semiconductors, electrons, holes and phonons.

**SHRINK-DOWN APPROACHES**

Introduction, CMOS Scaling, The nanoscale MOSFET, Finfets, Vertical MOSFETs, limits to scaling, system integration limits (interconnect issues etc.).

**TUNNELING TRANSISTORS AND OPTOELECTRONICS**

Resonant Tunneling Transistors, Single electron, transistors, new storage, optoelectronic, and spintronics devices.

**ATOMS-UP APPROACHES**

Molecular electronics involving single molecules as electronic devices, transport in molecular structures, molecular systems as alternatives to conventional electronics,

**MOLECULAR INTERCONNECTS AND BAND STRUCTURES**

Molecular interconnects- Carbon nanotube electronics, band structure & transport, devices, applications.

**REFERENCES**

1. Poole. C.P. Jr., Owens. F. J., Introduction to Nanotechnology, Wiley, 2003.
2. Waser Ranier, Nanoelectronics and Information Technology (Advanced Electronic Materials and Novel Devices), Wiley-VCH 2003.
3. Drexler. K.E., Nanosystems, Wiley 1992.
4. John H. Davies, The Physics of Low-Dimensional Semiconductors, Cambridge University Press, 1998

<b>ECE5119</b>	<b>MICROWAVE INTEGRATED CIRCUITS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
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### **INTRODUCTION TO MICROWAVE INTEGRATED CIRCUITS**

Introduction to Microwave Engineering and its concepts, Active and passive components.

### **ANALYSIS OF MICRO STRIP LINES**

Variation method, conformal transformation, numerical analysis- losses in micro strip lines- Slot line and Coupled lines-

### **DESIGN OF FILTERS AND COUPLERS**

Design of power dividers and combiners, directional couplers, hybrid couplers, filters.

### **COMPONENTS AND ELEMENTS IN MICS**

Micro-strip lines on ferrite and garnet substrates- Isolators and circulators- Lumped elements in MICS.

### **TECHNOLOGY OF MICS**

Monolithic and hybrid substrates- thin and thick film technologies, computer aided design.

### **REFERENCES**

1. Leo Young and Sobol., Advances in Microwaves, Vol.2, Academic Press Inc., 1974.
2. Bhat. B. and Koul. S., Stripline-like transmission lines for MICS, John Wiley, 1989.
3. Ishii. T.K., Handbook of Microwave Technology, Vol. 1, Academic Press, 1995.

<b>ECE 5120</b>	<b>VLSI TECHNOLOGY</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
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### **ENVIRONMENT FOR VLSI TECHNOLOGY**

Clean room and safety requirements, Wafer cleaning processes and wet chemical etching techniques. Impurity incorporation- Solid State diffusion modeling and technology- Ion Implantation modeling, technology and damage annealing- characterization of Impurity profiles.

### **OXIDATION**

Kinetics of Silicon dioxide growth both for thick, thin and ultra thin films. Oxidation technologies in VLSI and ULSI- Characterization of oxide films- High k and low k dielectrics for ULSI.

### **LITHOGRAPHY**

Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI- Mask generation.

### **CHEMICAL VAPOUR DEPOSITION TECHNIQUES**

CVD techniques for deposition of poly-silicon, silicon dioxide, silicon nitride and metal films- Epitaxial growth of silicon- modeling and technology.

Metal film deposition- Evaporation and sputtering techniques. Failure mechanisms in metal interconnects- Multi-level metallization schemes.

### **PLASMA AND RAPID THERMAL PROCESSING**

PECVD, Plasma etching and RIE techniques- RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits- Advanced MOS technologies.

**REFERENCES**

1. Chang, C.Y. and Sze, S.M., ULSI Technology, McGraw Hill Companies Inc, 1996.
2. Gandhi, S.K., VLSI Fabrication Principles, John Wiley Inc., New York, 1983.
3. Sze, S.M., VLSI Technology, McGraw Hill, 2<sup>nd</sup> Edition, 1988.

<b>ECE 6101</b>	<b>DESIGNING WITH ASICS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		3	0	0	3

**BASICS OF ASICS**

Types of ASICs, ASIC design flow, Programmable ASICs. Antifuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects.

**AN OVERVIEW OF ADVANCED FPGAS AND PROGRAMMABLE SOCS**

Architecture and configuration of Spartan II and Virtex II FPGAs. Apex and Cyclone FPGAs. Virtex II PRO kits and Nios kits, OMAP, ASIC physical design issues. System partitioning, interconnect delay models and measurement of delay. ASIC floor planning, placement and routing.

**DESIGN ISSUES IN SOC**

Design methodologies. Processes and flows. Embedded software development for SOC. Techniques for SOC testing. Configurable SOC, Hardware/software co design.

**HIGH PERFORMANCE ALGORITHMS FOR ASICS/ SOCS. SOC CASE STUDIES**

DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. **Case Studies-** Digital camera, Bluetooth radio/modem, SDRAM and USB controllers.

**TEXT BOOK**

1. Smith.M.J.S., Application Specific Integrated Circuits, Pearson, 2003.

<b>ECE 6102</b>	<b>FPGA BASED SYSTEM DESIGN</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
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**MULTIRATE SIGNAL PROCESSING**

Decimation and Interpolation. Spectrum of decimated and interpolated signals, Polyphase decomposition of FIR filters and its applications to multi-rate DSP. Sampling rate converters, Sub-band encoder.

**FILTER BANKS**

Uniform filter bank. Direct and DFT approaches. Introduction to ADSL Modem. Discrete multi-tone modulation and its realization using DFT. QMF. Computation of DWT using filter banks.

**DDFS**

ROM LUT approach. Spurious signals jitter. Computation of special functions using CORDIC. Vector and rotation mode of CORDIC. CORDIC architectures.

**BLOCK DIAGRAM OF A SOFTWARE RADIO**

Digital down converters and demodulators Universal modulator and demodulator using CORDIC. Incoherent demodulation - digital approach for I and Q generation, special sampling schemes. CIC filters. Residue number system and high speed filters using RNS.

Down conversion using discrete Hilbert transform. Under sampling receivers, Coherent demodulation schemes.

### **SPEECH CODING- SPEECH APPARATUS**

Models of vocal tract. Speech coding using linear prediction. CELP coder. An overview of waveform coding, Vocoders, Vocoder attributes. Block diagrams of encoders and decoders of G723.1, G726, G727, G728 and G729.

### **REFERENCES**

1. Mitra.S.K., Digital Signal processing, McGrawHill, 1998.
2. Reed. J H., Software Radio, Pearson, 2002.
3. Meyer.U., Baese, Digital Signal Processing with FPGAs, Springer, 2001.

<b>ECE 6103</b>	<b>ADVANCED COMPUTER ARCHITECTURE</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
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### **MULTIPROCESSORS AND PARALLEL PROCESSING APPLICATIONS**

Multiprocessors and multi-computers, Multi-vector and SIMD computers, PRAM and VLSI Models, Conditions of parallelism, Program partitioning and scheduling, Program flow mechanisms, Parallel processing applications, Speed up performance law.

### **SUPERSCALAR, VECTOR PROCESSORS AND MEMORY ORGANIZATION**

Advanced processor technology, Superscalar and vector processors, Memory hierarchy technology, Virtual memory technology, Cache memory organization, Shared memory organization.

### **PIPELINE PROCESSORS AND DESIGN**

Linear pipeline processors, Non linear pipeline processors, Instruction pipeline design. Arithmetic design, Superscalar and super pipeline design, Multiprocessor system interconnects, Message passing mechanisms.

### **MULTIVECTOR PROCESSORS AND MULTI-THREAD ARCHITECTURES**

Vector Processing principle, Multi-vector multiprocessors, Compound Vector processing. Principles of multi-threading, Fine grain multi-computers, Scalable and multithread architectures, Dataflow and hybrid architectures.

### **PARALLEL PROGRAMMING AND KERNEL ARCHITECTURE**

Parallel programming models, Parallel languages and compilers, Parallel programming environments, Synchronization and multiprocessing modes, Message passing program development. Mapping programs onto multi-computers. Multiprocessor UNIX design goals. MACH/OS kernel architecture, OSF/1 architecture and applications.

### **REFERENCES**

1. Hwang.K., Advanced Computer Architecture , TMH, 2001.
2. Stallings.W., Computer Organization and Architecture, McMillan, 1990 .
3. Quinn. M.J., Designing Efficient Algorithms for Parallel Computer, McGraw Hill, 1994.

<b>ECE 6104</b>	<b>FUZZY LOGIC AND NEURAL NETWORKS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
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### **INTRODUCTION TO FUZZY LOGIC**

Introduction to Fuzzy sets, Fuzzy relation, Approximate reasoning, Rules.

**FUZZY CONTROL DESIGN**

Fuzzy control design parameters, Rule base, data base, choice of fuzzification procedure, Choice of defuzzification procedure.

**TYPES OF FUZZY CONTROL**

Nonlinear fuzzy control, adaptive fuzzy control.

**INTRODUCTION TO NEURAL NETWORKS**

Biological Neurons, Artificial Neurons – various models,

**ARTIFICIAL NEURAL NETWORKS**

Various structures, Learning Strategies, Applications.

**REFERENCES**

1. Driankov.D., Hans.H., Michael.R., An Introduction to Fuzzy Control, Springer-Verlag, 1993.
2. Beale.R., Jackson. T.- Neural Computing - An Introduction, Adam Hilger, 1990.
3. Kosko.B., Neural Networks and Fuzzy Systems - A Dynamical System Approach to Machine Intelligence, PHI, 1994.

<b>ECE 6105</b>	<b>GENETIC ALGORITHMS AND VLSI DESIGN APPLICATIONS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
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**INTRODUCTION TO GA TECHNOLOGY**

Basics of GA Technology, Steady State Algorithm-Fitness Scaling-Inversion, GA for VLSI Design,

**PARTITIONING**

Layout and Test automation- Partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning

**PLACEMENT AND ITS ALGORITHM**

Hybrid genetic – genetic encoding-local improvement-WDFR-Comparison of Cas- Standard cell placement-GASP algorithm-unified algorithm.

**ROUTING AND ITS PROCEDURES**

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.

**POWER ESTIMATION AND FITNESS FUNCTION**

Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

**REFERENCES**

1. Pinaki Mazumder, E. M. Rudnick, Genetic Algorithm for VLSI Design, Layout and Test Automation, Prentice Hall, 1998.
2. Randy L.Haupt, Sue Ellen Haupt, Practical Genetic Algorithms, Wiley – Interscience, 1977.
3. Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco, Evolution Electronics- Automatic Design of electronic Circuits and Systems Genetic Algorithms, CRC press, 1<sup>st</sup> Edition, Dec 2001.

4. John R.Koza, Forrest H.Bennett III, David Andre , Morgan Kufmann, Genetic Programming Automatic programming and Automatic Circuit Synthesis, 1<sup>st</sup> Edition, May 1999

<b>ECE 6106</b>	<b>SYSTEM DESIGN</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
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### **INTRODUCTION TO SYSTEM HARDWARE DESIGN**

Basics of system hardware design, Hierarchical design using top-down and bottom-up methodology. System partitioning techniques, interfacing between system components.

### **SEQUENTIAL CIRCUIT DESIGN STYLES**

Handling multiple clock domains, Synchronous and asynchronous design styles, Interface between synchronous and asynchronous blocks, Meta-stability and techniques for handling it, interfacing linear and digital systems, data conversion circuits.

### **DESIGN OF STATE MACHINES**

Design of finite state machines, state assignment strategies. Design and optimization of pipelined stages. Use of data flow graphs, Critical path analysis, retiming and scheduling strategies for performance enhancement. Implementation of DSP algorithms.

### **SIGNAL INTEGRITY AND LAYOUT STRATEGIES**

Signal integrity and high speed behavior of interconnects- ringing, cross talk and ground bounce. Layout strategies at IC and board level for local and global signals. Power supply decoupling.

### **TEST STRATEGIES**

Border Scan, Built-In Self Test and signature analysis.

### **REFERENCES**

1. Jan M. Rabaey, Digital Integrated Circuits, Prentice Hall of India, New Delhi, 1997.
2. Smith.M.J.S., Application Specific Integrated Circuits, Addison Wesley, Reading -MA, 1999
3. Vijay K.Madiseti, VLSI Digital Signal Processing, IEEE Press , NY- USA, 1995

<b>ECE 6107</b>	<b>COMMUNICATION NETWORKS</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
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### **INTRODUCTION TO NETWORKS**

Packet Switching and Circuit Switching- Layered Network Architecture (OSI model).

### **POINT-TO-POINT PROTOCOLS AND LINKS**

Physical Layer, Error Detection and Correction, ARQ Retransmission Strategy, Framing, X.25 Standard.

### **QUEUEING THEORY AND DELAY ANALYSIS**

Little's Theorem, Analytical treatment of M/M/1 and M/M/m Queueing Systems, Simulation of queueing systems, Delay Analysis for ARQ System .

### **MULTI-ACCESS PROTOCOLS AND TECHNIQUES**

Aloha Systems, CSMA, IEEE-802 Standards. Routing and Flow Control. TCP/ IP Protocols, ISDN, ATM, Network Security.

**DESIGN OF LAN SYSTEM**

Design of a LAN System with commercially available functional units.

**REFERENCES**

1. Bertsekas.D. and Gallagar.R., Data Networks, PHI, 2<sup>nd</sup> Edition, 1992.
2. Stallings.W., Data and Computer Communication, Prentice-Hall, 1997.
3. Tanenbaum.A.S., Computer Networks , PHI, 3<sup>rd</sup> Edition, 1997.
4. Leon-Garcia and Widjaja. I., Communication Networks, TMH, 2000.

<b>ECE 6108</b>	<b>SIGNAL PROCESSING AND SMART ANTENNAS FOR WIRELESS COMMUNICATION</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
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**OVERVIEW OF WIRELESS AND MOBILE**

Cellular system concepts, standards and Evolution of mobile & wireless communication technologies.

**WIRELESS CHANNEL CHARACTERIZATION**

Attenuation, Shadowing, Fading, Doppler Shift, Delay Spread, Co-channel, Adjacent Channel and other forms of interferences.

**MODULATION TECHNIQUES**

QAM, Multi-tone, MSK, GMSK, CPM, TFM and OFDM Receiver architecture and algorithms- Digital IF receivers, Sub-sampling digital receivers, I & Q channel sampling, Non-coherent and Coherent techniques, Rake receiver.

**EQUALIZATION AND SYNCHRONIZATION**

MLSE, Adaptive Equalization- LMS, RLS & Blind adjustment, Timing recovery and carrier recovery. Smart Antennas systems- Generalized array signal processing, Beam forming concepts- DOB, TRB & SSBF, Switched beam antennas, spatial diversity, and fully adaptive antennas for enhanced coverage, range extension & improvement in frequency refuse, interference Nulling for LOS & Multi-path systems, SDMA concepts and Smart antennas implementation issues.

**RF ICs**

LNA, IQ Modulator, Mixers, DSPs & Micro-controllers in wireless communications, ASICs and FPGAs.

**REFERENCES**

1. Rappaport.T.S., Wireless Communication- Principles & Practices , Prentice Hall, 2<sup>nd</sup> Edition, 2002.
2. Liberti.J. and Rappaport.T.S., Smart Antennas for Wireless Communication- IS-95 and Third Generation CDMS applications, Prentice Hall, 1999.
3. Pattan. B., Robust Modulation Methods and Smart Antennas in Wireless communications, Prentice Hall, 2000.
4. Blogh.J.S. and Hanzo.L., Third-Generation Systems and Intelligent Wireless Networking- Smart Antennas and Adaptive Modulation, Wiley-IEEE Press, 2002.

<b>ECE 6109</b>	<b>LOW POWER PROCESSORS AND SOCs</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
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**LOW POWER PROCESSORS**

Techniques for power & process variation minimization, Low power DSP 's, Energy efficient Reconfigurable processors, Magic - a low power reconfigurable DSP, Low power asynchronous processors, Low power base band processors for communication

**LOW POWER MEMORIES**

Stand -by power reduction for SRAM memories, Low power cache design, Memory organization for low energy embedded systems

**LOW POWER SOC**

Power performance trade-off in design & SOCs, Low power SOC with power, Aware operating system generation, Low power data storage and communication for SOC, Network on chips of SOC interconnect.

**APPLICATIONS OF LOW POWER DESIGN, NETWORK AND ITS PROTOCOLS**

Highly integrated ultra-low power RF transceivers for wireless sensor networks, Power aware on demand, Routing protocols for mobile Ad HOC networks, Modeling computational, sensing and actuation surfaces

**EMEBDEDDED SOFTWARE**

Low power software techniques - low power /Energy compiler –Optimization - Design of low power processor cores using a retarget able tool - recent advances in low power design - Design & functional co verification Automation from the earliest system design Stages

**TEXT BOOK**

1. Christian Piguet, Low power Processors and SOCs.

<b>ECE 6110</b>	<b>VLSI SIGNAL PROCESSING TECHNIQUES</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
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**INTRODUCTION TO DSP**

Introduction to DSP Systems, Typical DSP algorithms- Pipelining and parallel processing, Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

**VLSI DSP SYSTEM DESIGN**

VLSI DSP technology current design, recent developments in the design of image & video processing ICs.

**HIGH PERFORMANCE DSP SYSTEMS**

High performance, Arithmetic for DSP systems, Pipelining & clocking of high performance synchronous digital systems.

**HIGH SPEED TRANSFORMS CODING ARCHITECTURES**

High speed transforms coding architectures for video communication, Design and programming of systolic array cells for signal processing.

**ANALOG VLSI SIGNAL PROCESSORS**

Analog VLSI signal processors, Switched capacitor parallel distributed processing network for speech recognition.

**TEXT BOOK**

1. Magdy A. Babyoumi and Earri E.Swarzlander, VLSI Signal Processing and Techniques, Kluwer Academic Publisher.